

**Optimized Self-Formed Barrier Layer for Scaled Hybrid Bonds**: At ECTC, IMEC researchers will describe the use of a self-formed MnOx barrier system in a 400nm pitch wafer-to-wafer hybrid bonding technology, in which a 60nm CuMn PVD seed is deposited directly after the hybrid pad etch. This technique makes it possible to omit a conventional Ta barrier deposition step, opening up the possibility to further reduce hybrid pitch pad scaling. By careful tuning certain critical process steps, among them the hybrid pad copper polish, high electrical yield on large hybrid bonded daisy chain structures was achieved. The researchers will discuss the results of their studies of dielectric breakdown, copper diffusion, Cu bulge-out and electromigration mechanisms of the self-formed barrier.

* **The graphs above** show electrical yield on hybrid bonded daisy chain structures as a function of pad pitch (400nm, 500nm and 700nm) for (a) equal and (b) unequal pad size, with >100,000 links/chain. The open symbols refer only to Cu-clear CMP), while the solid symbols refer to extra barrier-like pad CMP. Poor electrical yield is obtained on the wafers that only received the Cu-clear hybrid CMP step. When the barrier-like CMP step is added to the polishing process, the yield increases to 100% in case where the hybrid connection consists of equally sized hybrid pads.

**(Paper 9.4, “*Self-formed Barrier using Cu-Mn Alloy Seed applied to a 400nm Pitch Wafer-to-Wafer Hybrid Bonding Technology*,” S. Van Huylenbroeck et al, IMEC)**